METHOD FOR FORMING JUNCTION OF SEMICONDUCTOR DEVICE

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The present invention relates to a method of forming a junction region in a semiconductor device by which a doped epi-silicon layer is used to form a source/drain junction at a cell area, in applying an elevated source/drain junction using a selective epitaxial technology to the device as the integration degree of the semiconductor device increases; and ion implantation process and thermal process are performed to form a source/drain junction at a peripheral circuit area with a nitride film being capped. Thus, as the elevated source/drain junction is applied, a contact margin can be obtained and also a contact resistance can be reduced, at the cell area, due to flattened gate during a subsequent process of forming a contact. Also, as the ion implantation process and the thermal processing process are performed with the nitride film being capped, the effects of diffusing dopants can be prevented and also a source/drain junction having a relatively low depth of junction can be formed, at the peripheral circuit area. Further, metal contamination that could occur upon implantation of ions can be prevented at it. As a result, the present invention can improve the characteristic of the junction at each of the cell area and the peripheral circuit area